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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/963,533	09/27/2001	Takao Arai	PF-2840/NEC/US/mh/B1	9250

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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Acti n Summary	Application No. 09/963,533	Applicant(s) ARAI, TAKAO	
	Examiner Johannes P Mondt	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group II, claims 1-14, drawn to a semiconductor device, in Paper No. 5, is acknowledged.

Information Disclosure Statement

The examiner has considered the items listed in the Information Disclosure Statement of Paper No. 3.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. ***Claims 5-7*** recite the limitation "said impurity diffused region" in lines 2, 1-2, 2 respectively. There is insufficient antecedent basis for this limitation in the claim. Furthermore, there are two claims 6, the latter one being indefinite if only by virtue of being numbered the same as the former one. For definiteness of statements the examiner has chosen the first claim 6 as claim 6.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application

published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

5. ***Claims 1, 3, 8, 10-11 and 13-14*** are rejected under 35 U.S.C. 102(e) as being anticipated by Aoki et al (6,229,188 B1). Aoki et al (cf. Figures 1 and 5) teach a channel region (the region underneath 9 in Figure 5, see column 3, lines 8-10; region 2A in Figure 1, see column 2, lines 30-31) of a depletion type lateral field effect transistor (see claim 1 of Aoki et al, column 4, lines 28-34), said channel region (region 2A for Figure 1: cf. column 2, lines 20-40, and epitaxial doped region 9 in Figures 5: cf. column 3, line 30) of first conductivity type being selectively provided in a semiconductor region 1 of second conductivity type (cf. column 2, lines 20-40), and said channel region underlying a gate insulating film (region 10 in Figure 5, regions 2B and 5 in Figure 1), wherein an interface of said channel region to said gate insulating film lies at a lower level than an upper surface of said semiconductor region (cf. column 2, lines 30-31). In conclusion, Aoki et al anticipate claim 1.

With regard to claim 3: in view of claim 1 the channel region is of first conductivity type, while whether this conductivity type is achieved by diffusion or by ion implantation is irrelevant to the device but instead pertains to aspects of method of making the device; while it is inherent to the doping concentration of said channel region to be used for a threshold voltage adjustment if needed. The further limitation of claim 3 is thus seen not to distinguish over the prior art.

With regard to claim 8: Aoki et al teach (cf. Figures 1 and 5) a depletion type lateral MOS field effect transistor comprising: a channel region (2A in Figure 1 and

region underneath gate oxide region 10 in Figures 5, region 9 in Figures 5) of first conductivity type being selectively provided (by doping) in a semiconductor region of second conductivity type (cf. column 2, lines 20-40 and column 3, lines 5-40); source and drain regions of first conductivity type being selectively provided in said semiconductor region (regions 3 and 4 in Figure 1, regions 5 in Figures 5), said channel region being interposed between said source and drain regions (inherent in lateral MOSFET); a gate insulating film (5 in Figure 1, 10 in Figures 5) extending over said channel region; and a gate electrode (6 in Figure 1, 11 in Figures 5) provided on said gate insulating film, wherein an interface of said channel region to said gate insulating film lies at a lower level than an upper surface of said semiconductor region.

With regard to claim 10: in view of claim 8 the channel region is of first conductivity type, while whether this conductivity type is achieved by diffusion or by ion implantation is irrelevant to the device but instead pertains to aspects of method of making the device; while it is inherent to the doping concentration of said channel region to be used for a threshold voltage adjustment if needed. The further limitation of claim 10 is thus seen not to distinguish over the prior art.

With regard to claim 11: Aoki et al teach (cf. Figures 1 and 5) a semiconductor wafer including: an impurity-doped region of first conductivity type (2A in Figure 1, 9 in Figures 5) being selectively provided in a semiconductor region 1 of second conductivity type; and an oxide film (5 in Figure 1, 10 in Figures 5) overlying said impurity diffused region, wherein an interface of said impurity diffused region to said oxide film lies at a lower level than an upper surface of said semiconductor wafer (cf. column 2, lines 30-31

for Figure 1; cf. column 3, lines 5-10, for Figures 5). The foregoing does not exhaust the teaching by Aoki et al of the limitation of claim 11:

Specifically, in the alternative, Aoki et al also teach (cf. Figures 5) a semiconductor wafer 1 with an impurity-doped region "N+" of first conductivity type being selectively provided in a semiconductor region of second conductivity type; and oxide film 2 (cf. column 3, lines 10-15) overlying said impurity-doped region marked "N+", wherein an interface of said impurity-doped region to said oxide film lies at a lower level than an upper surface of said semiconductor wafer. In conclusion Aoki et al anticipate claim 11.

With regard to claim 13: in view of claim 11 the channel region is of first conductivity type, while whether this conductivity type is achieved by diffusion or by ion implantation is irrelevant to the device but instead pertains to aspects of method of making the device; while it is inherent to the doping concentration of said channel region to be used for a threshold voltage adjustment if needed. The further limitation of claim 13 is thus seen not to distinguish over the prior art.

With regard to claim 14: in the second, alternative teaching of claim 11 by Aoki et al, said oxide film has a thickness of 6,000 Å.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. ***Claims 2, 4, 12*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al (6,229,188 B1) in view of Vo et al (5,424,226).

With regard to claims 2 and 12: As detailed above, claims 1 and 11 are anticipated by Aoki et al. Aoki et al do not necessarily teach the further limitation of claims 2 casu quo claim 12, however, it would have been obvious to include the teaching of said further limitation in view of Vo et al,, who teach a depletion-mode NMOS within a CMOS device requiring the inclusion of a well (inherent in the CMOS concept; see column 1, lines 48-60). Motivation for including the teaching in this regard by Vo et al is the application of the invention by Aoki et al (improved threshold voltage determination) to the field of input noise reduction circuits (cf. column 1, lines 10-18). Combination of the inventions is easily accomplished, as the presence of a well within the substrate, in which the channel resides, in no way affects the manufacturing process of the buried channel aspects. Success in implementing the combination can therefore be reasonably expected.

With regard to claim 4: as is the case in CMOS devices, said well region as introduced in the invention of Aoki et al by implementing the teaching by Vo et al plays the role of the substrate underlying the channel region (see also, for instance, Wolf, ISBN 0-961672-4-5; pages 383-389) and therefore has a conductivity type opposite the first conductivity type of the channel region for this depletion-mode device, while, as discussed above, according to the teaching of Aoki et al said well region having an upper surface and including an impurity-doped region selectively provided in said well

region, said impurity-doped region being doped with an impurity of first conductivity type (namely: opposite the conductivity type of the well region), which impurity-doped region inherently can be used for adjusting the threshold voltage of said depletion type lateral field effect transistor, wherein said upper surface of said impurity-doped region lies at a lower level than said upper surface of said well region. Whether the impurity doping is achieved through diffusion or some other method such as ion implantation is irrelevant for the present device claim.

8. ***Claim 9*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al in view of Vo et al (5,424,226) and Wolf (ISBN 0-961672-4-5). As detailed above, Aoki et al anticipate claim 8. Aoki et al do not necessarily teach the further limitation of claim 9; however, it would have been obvious to teach the channel region of claim 8 wherein said semiconductor region comprises a well region selectively provided in an epitaxial layer of first conductivity type overlying the semiconductor substrate of first conductivity type, because depletion-mode CMOS devices form an obvious field of application for the invention of Aoki et al in view of the advantages of depletion mode CMOS devices as taught by Vo et al (see column 1, lines 10-18), while for the purpose of reliability at the sub-micron level twin-well CMOS devices are advantageous (see Wolf, page 388) and said wells are usually built on epitaxial substrates for the suppression of latchup in CMOS (see Wolf, page 385).

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nishinohara (6,465,842), specifically though not exclusively column 12, lines 15-40.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
November 14, 2002

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
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